3751
12-BIT A/D CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3751 is a twelve bit analog to digital converter using P channel enhancement mode MOS/LSI technology. The conversion is accomplished by the successive approximation technique. The word length is variable for eight, nine, ten or twelve bits by applying a DC potential to each of two control pins. The 3751 provides all the A/D system control functions such as: master timing, automatic start and recycle, and RZ or NRZ format control. By choosing the appropriate ladder network, the output will be in either a binary or binary coded decimal digital format.

FEATURES

- **8, 9, 10, OR 12 BIT WORD LENGTH**
- **RZ OR NRZ DIGITAL FORMAT**
- **COMPLETE LOGIC AND SYSTEM TIMING CIRCUITS INCLUDED ON THE CHIP**
- **BCD OVERVOLTAGE FLAG**
- **200 Ω TYPICAL "ON" RESISTANCE FOR THE TWO MSB**
- **500 Ω TYPICAL "ON" RESISTANCE FOR THE REMAINING TEN SWITCHES**
- **150 mW POWER DISSIPATION**
- **AUTOMATIC RESTART CIRCUITS**

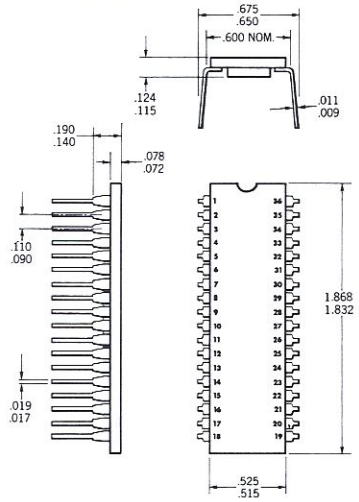
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

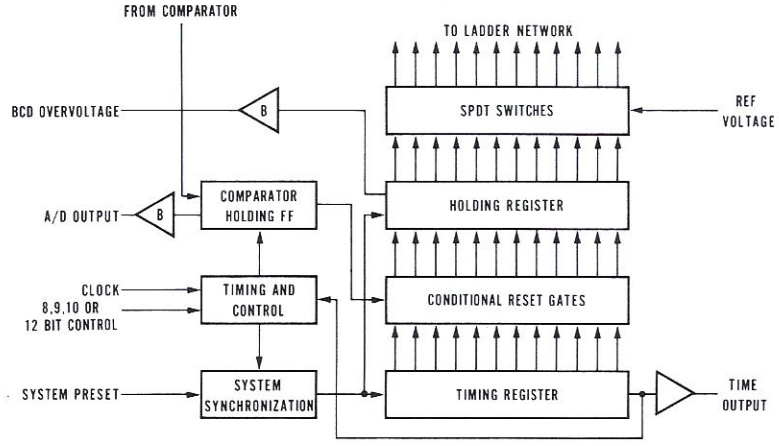
A/D Converters
Three Digit DVM's
Telemetry
Industrial Control
Computer Interface

PHYSICAL DIMENSIONS
36 PIN
DUAL IN-LINE PACKAGE

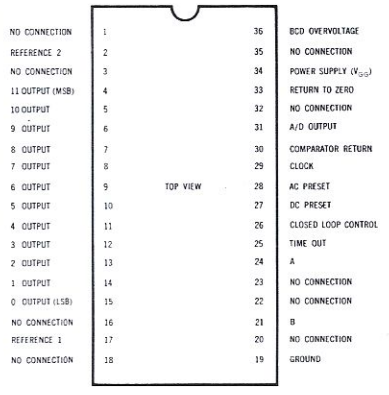


ORDER PART NO. A6H375114X

BLOCK DIAGRAM



PIN CONFIGURATION



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FAIRCHILD SEMICONDUCTOR
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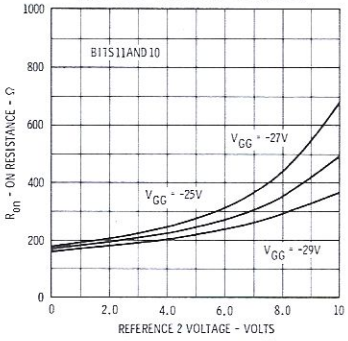
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10\ M\Omega$, $C_L = 10$ pF unless otherwise specified)

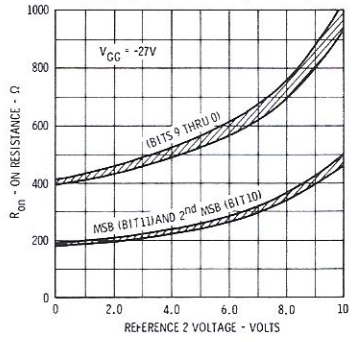
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
W_{cp}	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Bit Frequency	DC		250	kHz	
R_{ON}	MOS Switches					
	"11"	150	250	500	Ω	
	"10"	150	250	500	Ω	
	"9" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"11"		70	150	Ω	
	"10"		70	150	Ω	
	"9" thru "0"		120	250	Ω	
C_{IN}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient of Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
	Analog Switch Delay,					
t_{df}	rise and fall times		0.7		μs	$V_{GG} = -27$ V
t_f	(10% to 90% points)		0.5		μs	
t_{dr}			1.1		μs	
t_r			0.25		μs	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

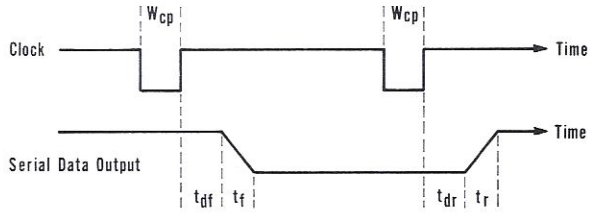


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



TIMING DIAGRAM

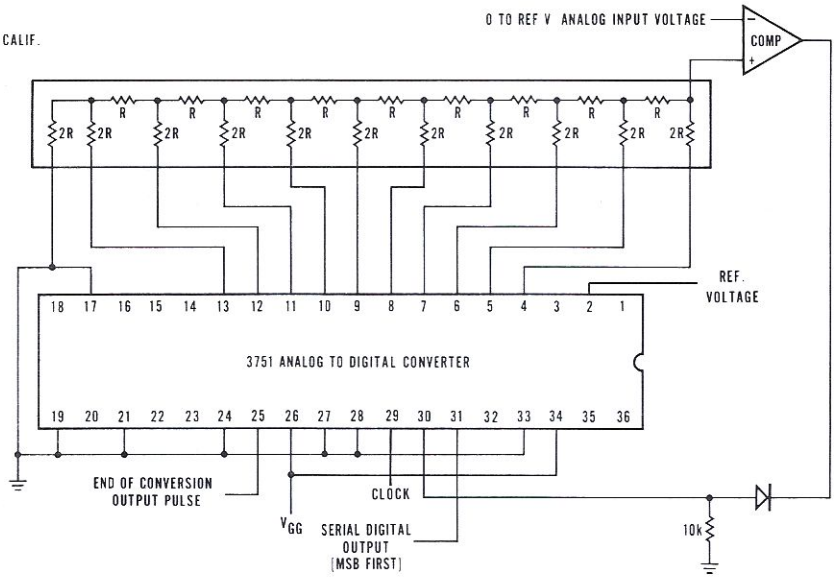
OUTPUT DELAY, RISE AND FALL TIMES



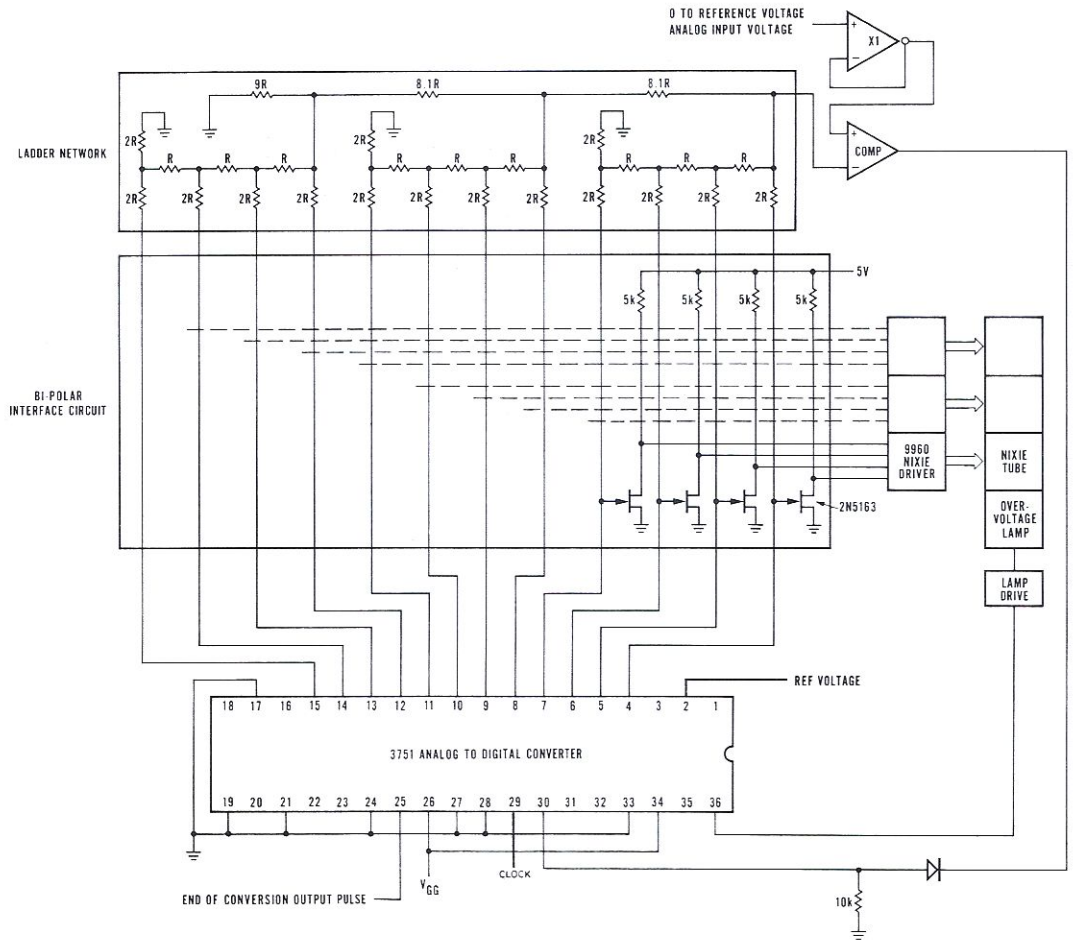
TEN BIT A/D CONVERTER

NO. OF BITS	R VALUE
8	12.5k
9	25k
10	50k
12	200k

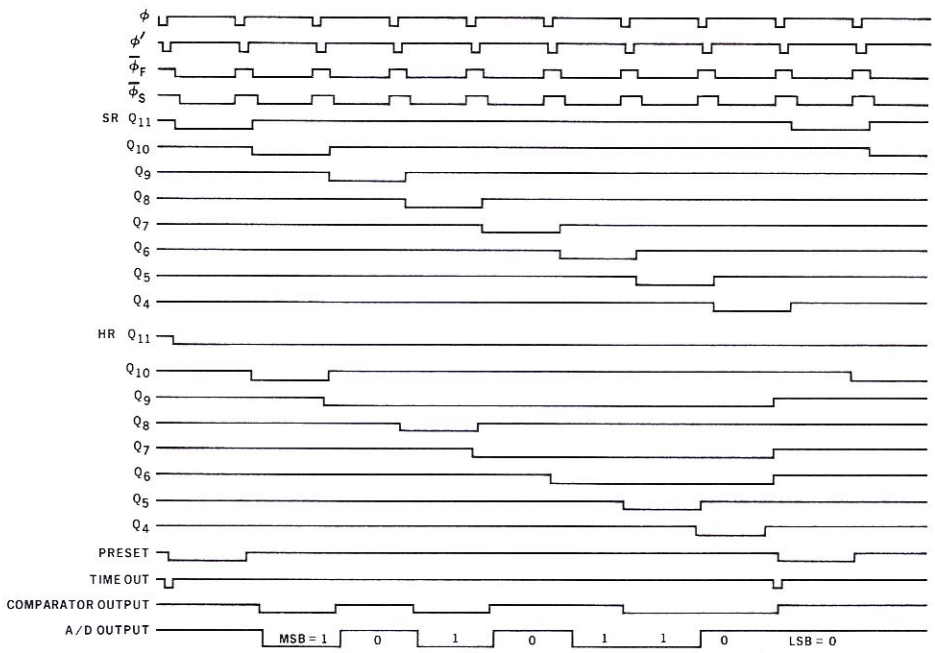
LADDER NETWORK MFGR'S
NEGADYNE CORP., ROCHESTER, N.Y.
ANGSTROM PRECISION INC., VAN NUYS, CALIF.


0 TO REF V ANALOG INPUT VOLTAGE
COMP
R
2R
REF. VOLTAGE
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
3751 ANALOG TO DIGITAL CONVERTER
19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
END OF CONVERSION OUTPUT PULSE
CLOCK
V_{GG}
SERIAL DIGITAL OUTPUT (MSB FIRST)
10k

THREE DIGIT BCD A/D CONVERTER



TYPICAL TIMING DIAGRAM



8 BIT FORMAT
ANALOG INPUT = −3.369 V = 10101100
REFERENCE VOLTAGE = −5.000 V
FIGURE 3

DESCRIPTION OF PIN FUNCTION

PIN NO.

24, 21 A, B: These two pins are connected as shown in the truth table below to control the length of the digital word.

	8	9	10	12
A	1	0	1	0
B	1	1	0	0

25 TIME OUT: A synchronous pulse with the clock is applied at this output at the end of each conversion. This pulse may be used to step a multiplexer or otherwise notify the system of the readiness of the A/D to start another conversion.

26 CLOSED LOOP CONTROL: A '1' voltage level continuously applied to this input will put the A/D in an automatic mode of operation. The time output pulse is internally gated to cause a preset at the end of each conversion and initiate a new conversion. The automatic start circuitry presets the circuit and restarts the conversion if a bit has been dropped in this mode of operation.

27 D.C. PRESET: A '1' voltage level applied to this input will cause an immediate preset and the unit will stay preset until this input is returned to a '0' voltage level.

28 A.C. PRESET: When a '1' level is applied to this input, the A/D is preset on the next clock pulse. The unit will continue to be preset on each clock pulse until the '1' level is removed from the input.

31 A/D OUTPUT: The serial digital conversion is available at this pin in a most significant bit (MSB) first format. The data output is delayed by one bit time.

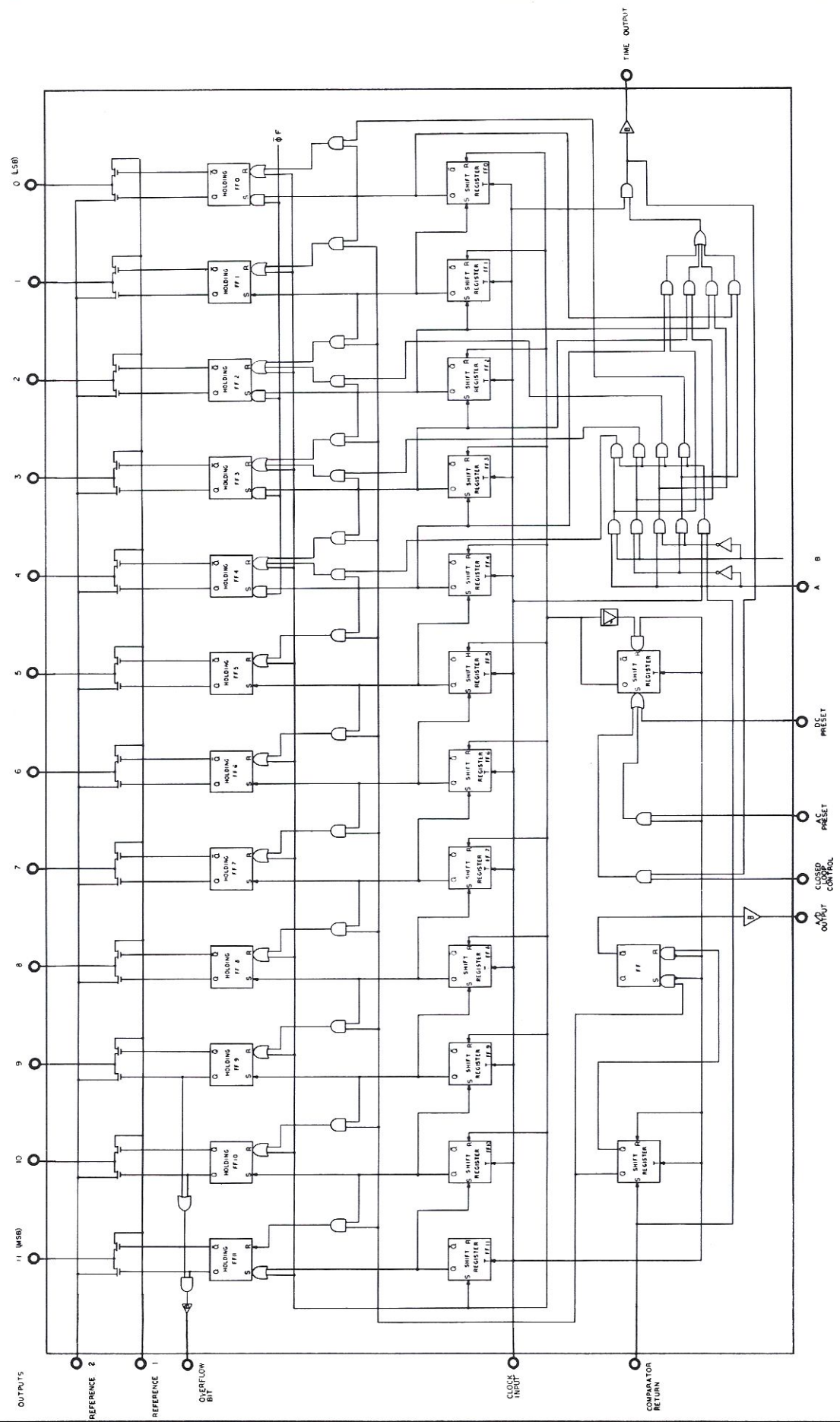
36 BCD OVERVOLTAGE: This output is used when a three digit analog to binary coded decimal (BCD) conversion is being made. If the binary equivalent of the most significant digit is greater than 9, a '1' voltage level is applied on this output.

33 RETURN-TO-ZERO: This input modifies the digital code format from non-return-to-zero (NRZ) to return-to-zero (RZ) if used. When tied to the clock line, the digital output will return to zero during each clock pulse. The RZ duty cycle can be varied by controlling the length of time that a '1' level is applied to this input.

30 COMPARATOR RETURN: The comparator output should be connected to this input. The input must be prevented from going positive with respect to substrate (ground). The output SPDT MOS switches are successively toggled to the reference voltage. This input will cause these switches to be conditionally reset if the ladder network output voltage is greater than the signal voltage.

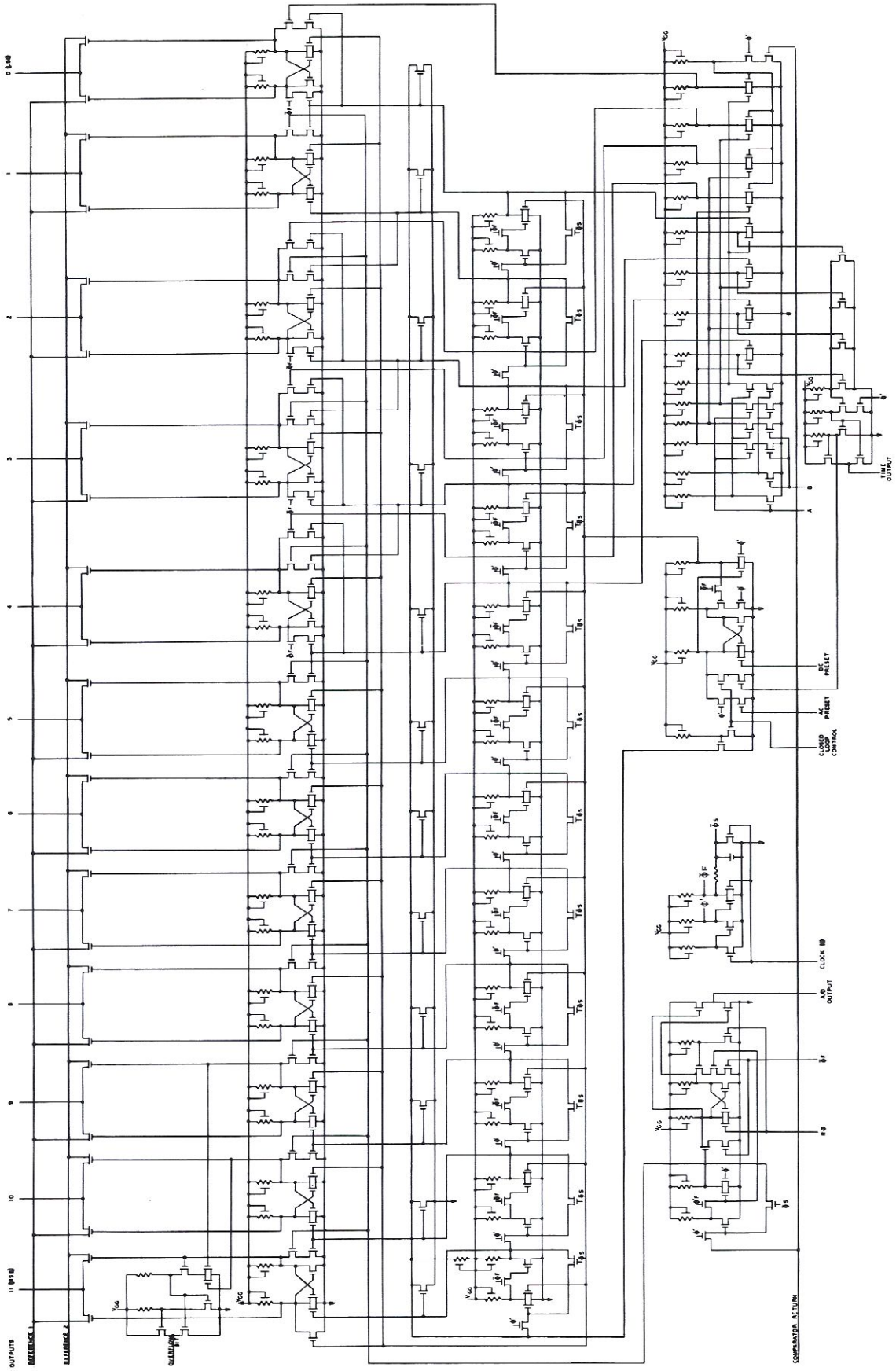
2, 17 REFERENCES 1 & 2: Reference 1 is normally connected to ground and reference 2 to −5.0 volts. However, they may each be connected anywhere between 0 and −5.0 volts D.C. for special applications.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



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